Understanding Self-Catalyzed Epitaxial Growth of III–V Nanowires toward Controlled Synthesis

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Supporting Information

ABSTRACT: The self-catalyzed growth of III–V nanowires has drawn plenty of attention due to the potential of integration in current Si-based technologies. The homoparticle-assisted vapor–liquid–solid growth mechanism has been demonstrated for self-catalyzed III–V nanowire growth. However, the understandings of the preferred growth sites of these nanowires are still limited, which obstructs the controlled synthesis and the applications of self-catalyzed nanowire arrays. Here, we experimentally demonstrated that thermally created pits could serve as the preferred sites for self-catalyzed InAs nanowire growth. On that basis, we performed a pregrowth annealing strategy to promote the nanowire density by enhancing the pits formation on the substrate surface and enable the nanowire growth on the substrate that was not capable to facilitate the growth. The discovery of the preferred self-catalyzed nanowire growth sites and the pregrowth annealing strategy have shown great potentials for controlled self-catalyzed III–V nanowire array growth with preferred locations and density.

KEYWORDS: Self-catalyzed nanowire growth, InAs, epitaxial, growth mechanism

With high mobility and low effective mass of carriers, III–V nanowires have been demonstrated as promising semiconductor channel materials for nanowire transistors.2−3 Heteroparticle catalysts, such as Au or Ni nanoparticles, have been successfully demonstrated for high-quality III–V nanowire growth.4−10 However, III–V nanowires produced by heteroparticle-catalyzed growth have shown the problem of thermal stability. Taking InAs nanowires as an example, at around 500 °C, the presence of Au catalysts promotes catalytic decomposition of InAs material greatly;11 besides, at 220–300 °C, Ni nanoparticles will react with semiconductor InAs nanowires to form fully conducted NiInAs nanowires.12 These effects of metal catalysts limit the processing temperature of III–V nanowires and nanowire-based devices. Additionally, to be compatible with current Si-based technologies, nanowires without Au nanoparticles are always preferred because Au can form deep-level traps in Si. Therefore, heteroparticle-free III–V nanowire growth methods are highly demanded for further applications and integrations in Si-based technologies. Here, we mainly focus on InAs nanowires because, among III–V nanowires, InAs nanowires have attracted particularly substantial attention due to the outstanding electrical performances.6,7,13−15

Different methods to achieve heteroparticle-free nanowire growth have been demonstrated for InAs nanowires. Selective area epitaxial growth of self-catalyzed InAs nanowires was performed on SiO2–Si and SiO2–InAs substrates with prepatterning and wet-etching steps to define the growth sites for nanowires.16,17 van der Waals epitaxial growth of InAs nanowires was also reported on mechanically exfoliated and chemical vapor deposition grown graphene,18,19 in which ledges, kinks, and defects were considered as preferred nucleation sites. However, these methods often require complex additional pregrowth steps, such as predeposition and patterning of SiO2 layer, transfer of graphene, etc., which make the whole process challenging for large-scale production. At the same time, the homoparticle-assisted vapor–liquid–solid (VLS) growth mechanism has been shown as applicable for self-catalyzed InAs nanowire growth on Si and III–V substrates without prepatterning steps being required.20−27 However, understandings of the preferred sites for this homoparticle-assisted self-catalyzed InAs nanowire growth are still very little, which limits the controlled synthesis and further applications of these self-catalyzed nanowires, particularly in the applications requiring position and density controls.

In our work, epitaxial self-catalyzed InAs nanowire growth was performed directly on III–V substrates. The distinct growth behaviors of epitaxial self-catalyzed InAs nanowires on different III–V substrates, especially InAs, GaSb, and GaAs, were compared. We found that thermally created pits observed on III–V substrates were correlated to the self-catalyzed growth. Through cross-sectional transmission electron microscopy imaging of as-grown samples, such pits were confirmed as the preferred sites for nanowire growth. This new finding...
allows us to develop a pregrowth annealing strategy to promote nanowire density by creating more pits before growth. Through this strategy, we can also enable growth on the substrate that was previously not capable to facilitate the growth. Our results open the potentials for synthesis of self-catalyzed III–V nanowires with controlled locations and density.

Self-catalyzed InAs nanowire growth was performed in a simple vapor deposition system with a multizone tube furnace. InAs powder (99.9999% from Alfa Aesar) was placed in the upstream zone as the solid precursor. Growth was tested on different III–V substrates (from MTI Corporation), including InAs, GaSb, and GaAs. Prior to the growth, III–V substrates were cleaned by sonication in acetone, isopropyl alcohol, and ethanol. These cleaned substrates were placed in the downstream zone as growth substrates. The tube was evacuated, and a base pressure of a few mTorr was achieved before the growth starts. Next, the upstream zone (precursor) and the downstream zone (substrate) were heated to the desirable source temperature (820–850 °C) and substrate temperature (490–500 °C), respectively, under 2.2 Torr pressure conditions maintained by the carrier gas H2. The typical growth period was 45 min to 1 h.

Scanning electron microscope (SEM) was utilized to image as-grown samples. As shown in Table 1, InAs nanowire growth was observed on all the InAs and GaSb substrates (Figure 1a–d); however, there is no nanowire growth on GaAs substrates, which will be further discussed later. All of the nanowires are grown along <111>B directions. The diameters of nanowires are in the range of 20–100 nm, and the length is up to 1 μm for 45 min growth. Transmission electron microscope (TEM) equipped with energy-dispersive X-ray spectrometer (EDX) was used to confirm the composition of nanowires (Figure 1e,f). For nanowires grown on all the III–V substrates tested, the In-to-As ratio in nanowires was confirmed as about 1:1. As shown in Figure 1g, high-resolution TEM (HRTEM) images taken on nanowires also confirm the zinc blende crystal structure with lattice constant of about 0.606 nm, which is consistent with the bulk value of InAs.

Growth on GaSb (111)A was studied in details to identify the preferred sites of the self-catalyzed InAs nanowire growth. SEM snapshots were taken on the GaSb substrate surfaces before growth and at different growth time. Before loading the substrate to the growth furnace, the surface of the GaSb (111)A substrate was smooth without any features observed (Figure 2a). At 5 min after all of the zones achieve the desired temperature, there was no nanowire, but there were pits observed all over the substrate surface (Figure 2b). The formation of these pits is due to the thermal annealing effect under the growth temperature in the first 5 min. At 45 min of growth, there are nanowires observed on GaSb (111)A substrate, as shown in Figure 1b. After removing the nanowires from this substrate by 10 min sonication in ethanol, there are also pits observed on the remaining substrate surface (Figure 2c). We estimated the pit density after 5 min of growth, the nanowire density after 45 min of growth, and the pit density after the removal of the nanowires. The results are compared in Figure 2d, indicating that these density values are correlated. Therefore, we hypothesized that thermally created pits on the substrate surface can be the preferred sites for InAs nanowire growth. A proposed growth process is illustrated in Figure 3. Within the initial several minutes under the growth temperature, there are pits formed on substrates due to the thermal annealing effect (Figure 3b). Due to capillary condensation, these pits serve as preferred sites to absorb indium droplets (Figure 3c). Then InAs nanowire growth was catalyzed by these indium droplets (Figure 3d).

As shown in Table 1, in addition to InAs and GaSb substrates, growth tests were also performed on GaAs (111)B substrates. At the identical growth condition, there was no nanowire growth observed on GaAs (111)B substrate. SEM images of GaAs as-grown samples after the 45 min growth show that the substrate surface is smooth without any pits (Figure S1). This could be due to the high melting point of GaAs (1238 °C), and thus, the growth temperature (490–500 °C) is not high enough to thermally evaporate the GaAs material surface to create pits before growth. Consequently, there is no nanowire growth. These results support our hypothesis that pits created on the substrate surface can be the preferred sites for InAs nanowire growth. On the basis of this observation, we expect that introducing pits through a pregrowth thermal annealing step at a suitable temperature could promote the InAs nanowire growth on the GaAs substrate.

Selected-area annealing was performed on GaAs (111)B substrate to demonstrate the promotion of the InAs nanowire growth through pits formation. Sample preparation process was illustrated in Figure 4a. A 20 nm SiO2 layer was deposited on part of the GaAs (111)B substrate surface (area A). The other part of the GaAs substrate was covered by a Si substrate during the deposition; thus, there is no SiO2 layer deposited in this area (area B). Prior to the annealing step, the substrate surface in the both areas were observed to be clean without any features (Figure S2a,b). The entire substrate was then thermally annealed in 20 sccm H2 at 650 °C for 5 min. The SiO2 layer protected the substrate surface in area A from being evaporated in the annealing step. Thus, the area A was still clean with no features observed, and high-density pits were observed only in area B. (Figure S2c,d) The pits formatted are in irregular shape, which is consistent with a previous report. The SiO2 layer was then completely removed by etching in buffered oxide etch (BOE) for 25 s. Low-density pits were observed in area A, which might be created in the etching step. In comparison, the formation of the higher density pits observed in area B was mainly due to the enhanced surface evaporation in the annealing step (Figure 3c). The self-catalyzed InAs nanowire growth was then performed on the substrate prepared, resulting in low-density nanowires in area A (Figure 3d) and high-density nanowires in area B (Figure 3e). We notice that the lengths of the high-density nanowires in area B are usually short, which might be attributed to the competition of source elements between nanowires, similar to a previous reported result. The direct correlation between the density of pits and the density of nanowires on the corresponding areas supports our hypothesis and suggests that the designed fabrication and creation process of pits could promote self-catalyzed InAs

### Table 1. Self-Catalyzed InAs Nanowire Growth on Different Substrates

<table>
<thead>
<tr>
<th>Substrates</th>
<th>Melting T °C</th>
<th>NW Growth</th>
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<tbody>
<tr>
<td>InAs (111)B</td>
<td>942</td>
<td>yes</td>
</tr>
<tr>
<td>InAs (111)A</td>
<td>712</td>
<td>yes</td>
</tr>
<tr>
<td>GaSb (111)A</td>
<td>1238</td>
<td>no</td>
</tr>
<tr>
<td>GaSb (110)</td>
<td>926</td>
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Nano Letters
nanowire growth on the substrate, which was not capable to facilitate the growth.

A key in our hypothesis is that the indium droplets condensed in the pits initiated the nanowire growth. Noticeably, in the TEM image shown in Figure 1c, in which the TEM sample was prepared through dispersion of sonicated nanowires from as-grown substrates, no obvious contrast indicated In droplets on tips of grown nanowires, which is attributed to the fact that these indium droplets were crystallized to be InAs during the final stage of nanowire growth, as reported previously.21 To directly confirm the presence of pits for nanowire growth, we have carried out the cross-sectional TEM study of as-grown samples. Cross-sectional TEM samples were prepared using a focused ion beam (FIB) liftout method (Note S1) from the area B of GaAs (111)B substrates as shown in Figure 4. Protective layers of Pt−C were deposited locally in the area of interest to avoid surface damage.

In the TEM images for the cross-sectional sample (Figure 5a), the InAs nanowire (indicated in the figure), the amorphous Pt−C layer, and the GaAs substrate (the region below the dashed white straight line) were identified. The Moiré patterns (indicated in the figure and circled by the dashed line) below the nanowire area were identified to have a horizontal spacing of 2.5−2.6 nm and a vertical spacing of about 3 nm, which are expected for InAs and GaAs lattices with overlap of (113) (horizontal) and (220) planes (vertical), respectively (Note S2). Such pattern outlines a pit area filled by the InAs material inside the GaAs substrate. As we observed in TEM for different nanowires, there was always a pit area with Moiré patterns at the root of each nanowire (Figure S3), which were all identified as formed by overlapping InAs and GaAs lattices. Notably, a small area of Moiré patterns was also observed at the bottom part of the nanowire, which is attributed to the fact that the observation direction is a little tilt away from the cross-sectional view; therefore, there is a small overlap of the GaAs substrate with the root of the InAs nanowire.

From the TEM images, the average depth of the pits was identified as about 52.30 ± 4.13 nm. As shown in Figure 5b,c, the depth of representative pits on a GaAs substrate after annealing at the same condition was measured to be 48.10 ± 5.96 nm by atomic force microscopy (AFM), consistent with the observation in the TEM images (Figure 5d). More AFM images showing the pits depth are illustrated in Figure S4. The pits with similar sizes on the annealed GaAs substrates were also reported previously.29 Additionally, in the EDX elemental mapping carried out in the scanning TEM (STEM) mode, an area consisted of indium, gallium, and arsenic was observed at the root of a nanowire from the cross-sectional sample, which was identified as the pit area (Figure S5). These results confirm our hypothesis that the pits are the preferred sites for the nanowire growth and support that the pregrowth annealing step enhanced the nanowire growth by creating pits on the substrate surface.

We have demonstrated the pregrowth annealing method as an effective method to promote nanowire growth on GaAs substrates based on the formation of pits as the preferred sites.

Figure 1. Self-catalyzed InAs nanowire growth on (a) InAs (111)B substrate (85° tilt view, inset is the 70° tilt view), (b) InAs (111)A substrate (top view), (c) GaSb (111)A substrate (top view), and (d) GaSb (110) substrate (top view). The insets in panels b−d show projections of three <111> B directions of the substrate. (e) TEM image of an InAs nanowire and (f) EDX spectrum taken from it showing In and As peaks, in which Fe and Cu peaks are from pole pieces in the TEM column and the TEM grid. (g) High-resolution TEM image of InAs nanowire with growth direction of <111> B. B: zone axis. The inset shows fast Fourier transform (FFT) of the TEM image. Scale bars are (a) 400 nm; inset of (a) 400 nm; (b) 800 nm; (c) 1 μm; (d) 2 μm; (e) 500 nm; and (g) 5 nm.
We also tested this strategy on InAs (100) substrates. Here, the pregrowth annealing step was carried in 20 sccm H₂ and 500 °C for 2 min. Growth conditions were kept identical. Figure 6 shows SEM images taken from as-grown samples without (Figure 6a) and with (Figure 6b) the pregrowth annealing step. Specifically, the nanowire density was estimated and compared in Figure 6c, showing ~0.3/μm² for the sample without annealing and ~4.5/μm² for that with annealing. Our results
Figure 4. Self-catalyzed InAs nanowire growth on GaAs (111)B substrates after selected-area annealing. (a) Schematic of substrate preparation and growth process. Areas A (left) was deposited by a SiO₂ layer, and area B (right) was not deposited. (b,c) SEM images taken from areas A (b) and B (c) of the as-prepared substrate after removal of SiO₂ through 25 s etching in BOE solution (top view). The locations of the pits in (b) are indicated by the white arrows. The pits’ locations in (c) are not marked because the pits are with obviously high-density. (d) and (e) SEM images taken from areas A (d) and B (e) of the as-grown sample (20° tilted view).

Figure 5. Direct observation of the pits. (a) Cross-sectional TEM image on the sample made from area B shows InAs nanowire, GaAs substrate (below the white straight dash line), and the pit area. (b,c): AFM analysis on the tomography of annealed GaAs substrate surface. (d): Comparison between the average depths measured from TEM and AFM, respectively (each method having ~10 pits). Scale bars are (a) 20 and (b) 200 nm.
suggest that such a preannealing step is applicable for InAs substrates for the promoted self-catalyzed InAs nanowire growth and offers a convenient way to greatly improve the density of InAs nanowires.

In conclusion, self-catalyzed InAs nanowire growth was demonstrated on varieties of III–V substrates. Thermally created pits on the substrate surface were supposed to provide preferred sites for self-catalyzed InAs nanowire growth. However, even though nanowire growth was observed on all InAs and GaSb substrates, no growth was found on the GaAs (111)B substrate, which was due to few thermally created pits on the substrate. Selected-area growth with a pregrowth annealing step on the InAs (100) substrate con- demonstrates on varieties of III–V substrates. Thermally this work was supported by Army Research Office grant no. 57975-EL. The authors gratefully acknowledge Dr. Sammy Saber for help in the TEM sample preparation.

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Additional SEM, TEM, AFM images; a scanning TEM image with elemental mappings; cross-sectional TEM sample preparation by FIB; and identification of the Moiré patterns. (PDF)

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